

REMARKS

The specification has been amended to replace the Attorney Docket Number with the corresponding U.S. Patent Application Serial Number.

Applicants wish to thank the Examiner for responding to the telephone inquiry of November 13, 2002 regarding a discrepancy between the Office Action Summary sheet and the Detailed Action section of the Office Action. The Office Action Summary sheet indicates that Claim 10 is objected to while the Detailed Action, at page 6, indicates that Claim 11 is objected to.

In the return phone message of November 14, 2002, the Examiner stated that the Office Action Summary sheet is in error and that Claim 11 is the claim objected to. The Examiner further indicated that a change has been entered into the record to correct the error on the Office Action Summary sheet. However, Applicants note that Claim 11 is rejected at pages 3 and 5 of the Detailed Action. Further, there is no rejection of Claim 10 in the Detailed Action. Accordingly, Applicants request further clarification about whether Claim 10 or Claim 11 is objected to in the next communication from the United States Patent and Trademark Office.

The sections below are numbered to correspond with the paragraph numbering used by the Examiner in the Office Action.

2/3/4. Claims 1 and 5 are novel over Bigler et al. (USPN 4,760,440)

Regarding Claim 1, the Examiner states:

... Bigler discloses a semiconductor process as claimed. See FIG. 2 where Bigler teaches a method comprising:

***forming a central aperture 14 in a substrate;
forming an electrically conductive trace 26 on a first surface of said substrate, said trace comprising a tab ...***

(Office Action, page 2, **bold** and underline in original, **bold italic** emphasis added).

The Examiner's statement is respectfully traversed. In the Abstract, Bigler et al. generally teaches:

A package for solid state image sensor devices, such as CCD image sensors, includes a base plate on which a plurality of the image sensor devices are mounted in end-to-end abutting relation with the detector arrays of the image sensors being over an opening in the base plate, (Title page Abstract, emphasis added).

More specifically, at col. 1, lines 54-62, Bigler et al. teaches:

A package for solid state image sensors includes a base of silicon having a flat surface and an opening therethrough. A plurality of CCD image sensor devices are mounted on the flat surface of the base in close proximity to each other. Each of the image sensor devices includes a silicon substrate having an array of detectors thereon. The image sensors are mounted on the base with the detector array being exposed through the opening therein.
(Emphasis added).

Further, as can best be seen with reference to FIG. 2, Bigler et al. teaches:

... The package 10 includes a **flat, rectangular base plate 12** of polycrystalline silicon. **The base plate 12 has a narrow opening 14 therethrough** which extends longitudinally along a portion thereof.
(Col. 2, lines 10-13, emphasis added).

Finally, at col. 2, lines 52-55, Bigler et al. teaches:

Each of the image detector devices 24 is secured to the surface 16 by a layer 26 of silver filled epoxy.
(Emphasis added).

Thus, Bigler et al. teaches that **image detector devices 24, are secured by a "layer 26" of epoxy on surface 16 of "base plate 12", and over a "narrow opening 14",** asserted to be a central aperture, through base plate 12.

In stark contrast Claim 1 recites:

A method comprising:
 forming a central aperture in a substrate;
 forming an electrically conductive trace
on a first surface of said substrate, said
trace comprising a tab; and
 **supporting an image sensor in said central
aperture by said tab.**

Applicants respectfully submit that the Examiner does not call out where Bigler et al. includes "supporting an image sensor in said central aperture" as recited in Claim 1. Applicants submit that, as shown above, Bigler et al. actually teaches away from this feature of Applicants invention, as recited in the Claim, since the **image detector devices** of Bigler et al. are described as being **on** the flat surface of **the base support "over" and not "in" a narrow opening** through the base.

Accordingly, Applicants submit that Claim 1 is allowable over Bigler et al. In addition, Claim 5 depends directly from Claim 1, and is therefore allowable for at least the same reasons as Claim 1.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

5/6/7/8. Claims 2-4 satisfy 35 U.S.C. §112, 2nd paragraph.

The Examiner states:

Claim 2 recites the limitation "said trace sealing" in line 13. There is insufficient antecedent basis for this limitation in the claim. (Office Action, Page 3.)

The Examiner's statement is respectfully traversed.

Claim 1 recites:

A method comprising:
forming a central aperture in a substrate;
forming an electrically conductive trace on a
first surface of said substrate, **said trace**
comprising a tab; and
supporting an image sensor in said central
aperture by said tab. (Emphasis added).

Claim 2 recites:

The method of Claim 1 further comprising
forming an interconnection ball aperture in said
substrate, an end of **said trace sealing** said
interconnection ball aperture at said first surface
of said substrate. (Emphasis added).

Applicants direct the Examiner's attention to the
specification at page 2, lines 25-26, which sets forth:

Further, ends of **the traces seal** the interconnection
ball apertures at the lower surface of the
substrate. (Emphasis added).

Applicants also direct the Examiner's attention to the
specification at page 12, lines 13-20, which sets forth:

Referring now to FIGS. 6 and 7 together, trace
regions 520 of sheet 402 (FIG. 5) form traces 114.
Tabs 116 of traces 114 project below and under hang
central apertures 106 of substrates 102. Further,
second ends 124 of **traces 114 cover and seal**
interconnection ball apertures 122 at lower surface
202L of image sensor substrate 202, and more
generally, and lower surfaces 102L of substrates
102. (Emphasis added).

Applicants respectfully submit that one of skill in the
art would understand what is being claimed in Claim 2 when read
in light of the specification.

Accordingly, Claim 2 satisfies 35 U.S.C. 112, second
paragraph. Claims 3 and 4, which depend, directly or

indirectly, from Claim 2, also satisfy 35 U.S.C. 112, second paragraph, for at least the same reasons as Claim 2.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

9/10. Claims 6-9, 11, and 12 are patentable over Bigler et al. (USPN 4,760,440) in view of Peterson et al. (USPN 6,384,473 B1)

As noted above in Section 2/3/4., Claim 1 is allowable over Bigler, et al. Peterson et al. does not cure the deficiencies in Bigler, et al. and in fact teaches away from the method recited in Claim 1, from which Claims 6-9, 11, and 12 directly or indirectly depend.

For example, Peterson et al. teaches:

FIG. 3A shows a schematic cross-section view of a first example of a microelectronic package 8 for housing at least one microelectronic device according to the present invention, comprising a hollow assembly 10 of stacked, electrically insulating plates. ... Assembly 10 further comprises a first plate 16. Plate 16 has a first surface 20, an opposing second surface 18, and a first aperture 22 through plate 16. Plate 16 also has an electrically conductive metallized trace 24 disposed on surface 18, for conducting an electrical signal between interior interconnect location 12 and exterior interconnect location 14. (Col. 6 , lines 39-53, emphasis added).

Thus, Peterson et al. teaches that metallized trace 24 is disposed on surface 18, i.e., the upper surface of plate 16. Further, at col. 6, lines 57-62, Peterson et al. teaches:

In FIG. 3A, assembly 10 further comprises a second plate 30, which has a third surface 34, an opposing fourth surface 32, and a second aperture 36 through plate 30 for providing physical access to insert device 100 into package 8. Surface 18 of plate 16 is bonded to the surface 34 of plate 30 to form assembly 10.

Thus, Peterson et al. teaches that plate 30 is a separated plate from plate 16 and that plate 30 and plate 16 are bonded at their respective adjacent surfaces 34 and 18.

Taken together, the above citations and FIG. 3A of Peterson et al. teach that a microelectronic device is supported by a "metal trace 26" on the upper "surface 18" of first "plate 16" over and not in "aperture 22" of "plate 16".

Applicants respectfully submit that "plate 30" is a separate plate forming a cover for "plate 16". The Abstract of Peterson et al., for example, states that:

... The microelectronic device can be flip-chip bonded on the plate to these traces, and oriented so that the light-sensitive side is optically accessible through the window. **A cover lid can be attached to the opposite side of the package.** ... (Title page Abstract, Emphasis added).

With respect to another embodiment, Peterson et al. analogously teaches that:

In FIG. 3B, assembly 10 comprises twelve individual layers of ceramic tape stacked and laminated to form a monolithic, unitized body having an integral window 26. The part of assembly 10 grouped as plate 16' comprises six individual layers (e.g. sheets) of glass-ceramic tape (e.g. layers 61, 62, 63, 64, 65, and 66). Likewise, the part of assembly 10 grouped as plate 30' comprises six additional individual layers (e.g. layers 67, 68, 69, 70, 71, and 72). Each layer can be individually personalized with the appropriate inside and outside dimensions. **Metallized trace 24 can be deposited on the upper surface of layer 66 (corresponding to surface 18 of FIG. 3A) prior to stacking of the individual layers.** (Col. 9, lines 53-65, emphasis added).

Accordingly, Applicants respectfully submit that Peterson et al. teaches away from and the Examiner does not call out where Peterson et al. discloses, teaches, or suggests a method comprising:

forming a central aperture in a substrate;
forming an electrically conductive trace on a
first surface of said substrate, said trace
comprising a tab; and
supporting an image sensor in said central
aperture by said tab,

as recited in Claim 1, emphasis added.

Accordingly, Claim 1 is allowable over Bigler, et al. and Peterson et al., alone or in combination. In addition, Claims 6-9, 11, and 12 depend directly from Claim 1 and are therefore allowable for the same reasons as Claim 1.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

17/18. Claims 2-4, 10 or 11, and 13-21 - Allowable
Subject Matter.

Applicants note that the only rejection of Claims 2-4 is the 35 U.S.C. § 112, 2nd paragraph rejection. As shown above in Section 5/6/7/8., Claims 2-4 satisfy 35 U.S.C. §112, 2nd paragraph. Accordingly, Applicants assume that Claims 2-4 are allowable.

Applicants also note that, as shown in Section 2/3/4., Claim 1 is allowable. Claims 10 and 11 depend, directly or indirectly, from Claim 1 and are therefore allowable for at least the same reason as Claim 1.

The Examiner also states that Claims 13-21 are allowed.

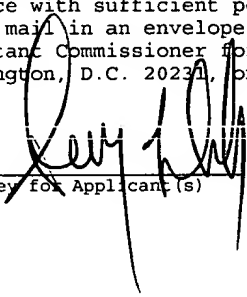
CONCLUSION

Claims 1-21 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating

to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

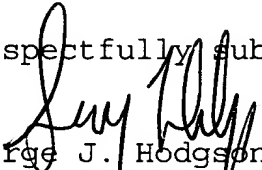
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 23, 2002.


Attorney for Applicant(s)

December 23, 2002
Date of Signature

Respectfully submitted,


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